What is claimed is:

Sub A1

1. A method of manufacturing a semiconductor memory device capable of electrically writing and erasing data, said semiconductor memory device having a plurality of cell transistors for storing data, each of said cell transistors having a floating gate electrode and a control gate electrode, and a plurality of select transistors for controlling and selecting said cell transistors, said method comprising the steps of:

before forming the control gate electrodes of said cell transistors, exposing a surface of a substrate directly above channel regions of said select transistors fabricated in the same process as the cell transistors;

forming gate insulating films of said select transistors on the exposed surface of the substrate; and

forming the control gate electrodes of said cell transistors and forming gate electrodes of said select transistors on said gate insulating films.

2. The method of manufacturing a semiconductor memory device according to claim 1, further comprising the step of:

simultaneously forming a first diffused layer serving as source and drain regions of said cell transistors and a second diffused layer serving as

insulating films of said select transistors have a film thickness which is the same as the film thickness of the gate insulating film of a transistor which requires a high withstand voltage, among the transistors of said peripheral circuit.

6. The method of manufacturing a semiconductor memory device according to claim 4, wherein the gate insulating films of said select transistors have a film thickness which is the same as the film thickness of the gate insulating film of a transistor which requires a high withstand voltage, among the transistors of said peripheral circuit.

7. A semiconductor memory device capable of electrically writing and erasing data, comprising:

a plurality of cell transistors for storing data, each of said cell transistors having a floating gate electrode and a control gate electrode; and

a plurality of select transistors for controlling and selecting said cell transistors, said select transistors having gate electrodes each comprising a single polysilicon film, said gate electrodes being formed simultaneously with the control gate electrodes of said cell transistors.

Sub A1 cont.

source and drain regions of said select transistors.

3. The method of manufacturing a semiconductor memory device according to claim 1, further comprising the steps of:

forming gate insulating films of transistors of a peripheral circuit comprising a logic operation circuit, simultaneously with the gate insulating films of said select transistors; and

forming gate electrodes of the transistors of said peripheral circuit simultaneously with the gate electrodes of said select transistors.

4. The method of manufacturing a semiconductor memory device according to claim 2, further comprising the steps of:

forming gate insulating films of transistors of a peripheral circuit comprising a logic operation circuit, simultaneously with the gate insulating films of said select transistors; and

forming gate electrodes of the transistors of said peripheral circuit simultaneously with the gate electrodes of said select transistors.

5. The method of manufacturing a semiconductor memory device according to claim 3, wherein the gate

8. The semiconductor memory device according to claim 7, wherein said cell transistors have source and drain regions comprising a first diffused layer, and said select transistors have source and drain regions comprising a second diffused layer, said first diffused layer and said second diffused layer being formed simultaneously with each other.

9. The semiconductor memory device according to claim 7, including a peripheral circuit comprising a logic operation circuit and having transistors, wherein said transistors of the peripheral circuit have gate insulating films formed simultaneously with gate insulating films of said select transistors, and gate electrodes formed simultaneously with the gate electrodes of said select transistors.

10. The semiconductor memory device according to claim 8, including a peripheral circuit comprising a logic operation circuit and having transistors, wherein said transistors of the peripheral circuit have gate insulating films formed simultaneously with gate insulating films of said select transistors, and gate electrodes formed simultaneously with the gate electrodes of said select transistors.

11. The semiconductor memory device according to claim 9, wherein the gate insulating films of said select transistors have a film thickness which is the same as the film thickness of the gate insulating film of a transistor which requires a high withstand voltage, among the transistors of said peripheral circuit.

12. The semiconductor memory device according to claim 10, wherein the gate insulating films of said select transistors have a film thickness which is the same as the film thickness of the gate insulating film of a transistor which requires a high withstand voltage, among the transistors of said peripheral circuit.

Add A2